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"no restriction is placed on positions of the clo

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Tip: Try removing quotes from your search to get more results.

Your search - **"no restriction is placed on positions of the clocked logic circuit and the non-clocked logic circuit"** - did not match any documents.

### Suggestions:

- Make sure all words are spelled correctly.
- Try different keywords.
- Try more general keywords.

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[Preferences](#)**Web**Results 1 - 5 of about 11 for "**basic units**" "**clocked logic circuit**". (0.35 seconds)

Tip: Save time by hitting the return key instead of clicking on "search"

**Method of fabricating an integrated circuit through utilizing ...**The method includes forming a plurality of **basic units** with the same component ... layout layer to program the **basic units** for building a **clocked logic circuit**.[www.freshpatents.com/Method-of-fabricating-an-integrated-circuit-through-utilizing-metal-layers-to-progra...](http://www.freshpatents.com/Method-of-fabricating-an-integrated-circuit-through-utilizing-metal-layers-to-progra...) - 26k - [Cached](#) - [Similar pages](#)**Method of fabricating an integrated circuit through utilizing ...**The method of claim 1 wherein step ( b ) utilizes the layout layer to program a plurality of **basic units** for generating the **clocked logic circuit** . ...[www.freshpatents.com/Method-of-fabricating-an-integrated-circuit-through-utilizing-metal-layers-to-progra...](http://www.freshpatents.com/Method-of-fabricating-an-integrated-circuit-through-utilizing-metal-layers-to-progra...) - 20k - [Supplemental Result](#) - [Cached](#) - [Similar pages](#)[ [More results from www.freshpatents.com](#) ]**METHOD OF FABRICATING AN INTEGRATED CIRCUIT THROUGH UTILIZING ...**The method includes forming a plurality of **basic units** with the same ... the **basic units** for building a **clocked logic circuit** and a **non-clocked logic** ...[www.patentdebate.com/PATAPP/20050186714](http://www.patentdebate.com/PATAPP/20050186714) - [Supplemental Result](#) - [Similar pages](#)**[PDF] Gate-diffusion input (GDI): a power-efficient method for digital ...**

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Given a **clocked logic circuit** with known Tcycle. and Tsetup, buffering of cascaded GDI ...consists of a cascade of four identical **basic units**, while the ...[ieeexplore.ieee.org/iel5/92/26463/01178080.pdf](http://ieeexplore.ieee.org/iel5/92/26463/01178080.pdf) - [Similar pages](#)**Logic circuit and method of logic circuit design - Patent 20040130349**[0159] Given a **clocked logic circuit** with known T.sub.cycle and T.sub.setup, ... **basic units**, while the comparison data is transmitted through the units. ...[www.freepatentsonline.com/20040130349.html](http://www.freepatentsonline.com/20040130349.html) - 156k - [Cached](#) - [Similar pages](#)*In order to show you the most relevant results, we have omitted some entries very similar to the 5 already displayed.**If you like, you can [repeat the search with the omitted results included](#).*Try [Google Desktop](#): search your computer as easily as you search the web.[Search within results](#) | [Language Tools](#) | [Search Tips](#) | [Dissatisfied? Help us improve](#)[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

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